

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

the Application of: HASHIMOTO, Hiroshi et al.

Serial No.: 09/960,399

Group Art Unit: 2814

Filed: September 24, 2001

Examiner: Howard Weiss

P.T.O. Confirmation No.: 5652

A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS For. HAVING COMPENSATED STRUCTURES TO REDUCE MANUFACTURING DEFECTS (as amended)

REQUEST FOR APPROVAL OF DRAWING CHANGES

Commissioner for Patents Washington, D.C. 20231

October 1, 2002

Sir:

The Examiner's approval of the drawing corrections indicated in red ink on the attached 51 sheets of drawings is respectfully requested.

Upon receipt of approval of the drawing corrections and a formal Notice of Allowance, a bonded draftsman will be retained and the appropriate corrections will be made.

In the event any fees are required in connection with this paper, please charge our Deposit Account No. 01-2340.

> Respectfully submitted, ARMSTRONG, WESTERMAN & HATTORI, LLP

Attorney for Applicant

Reg. No. 36,938

GNS/alw

Atty. Docket No. 011225 Suite 1000, 1725 K Street, N.W. Washington, D.C. 20006 (202) 659-2930

PATENT TRADEMARK OF

Attachment: 51 Sheets of Corrected Drawings